AMPLEON

ART (Advanced Rugged Technology) White Paper

Ampleon's advancements with ruggedized Si LDMOS transistors of up to 2 kW of RF Power for 1 through 400 MHz

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Overview

Ampleon recently released a series of rugged transistors, engineered specifically for the industrial, scientific and medical applications which offer robust VSWR ruggedness withstand while delivering the best in terms of RF power, gain and efficiency. We named this series "ART", short for "Advanced Rugged Transistor".

ART's novel Silicon LDMOS node was engineered to obtain a high drain-source breakdown while maintaining a compelling low output capacitance to allow for a rugged transistor with high transconductance in the frequency range from HF through UHF. The ART series has two versions: ART1K6 (50 V V_{DS} / 177 V V_{DS} minimum breakdown) and ART2K0 (65 V V_{DS} / 200 V V_{DS} minimum breakdown range). The high VDS breakdown offers the threshold for VSWR ruggedness features during 65:1 withstand conditions. Further, the low output capacitances allow for frequency ranges of up to 450 MHz with high gain and efficiency. The chart below provides a comparison of features to our popular BLF188XR (current generation in high volume production) and provides some perspective on comparison to the competitive landscape of devices.

Features	BLF188XR	ART1K6	ART2K0	Competitive LDMOS	Competitive VDMOS
V_{DS} (Max) Volts	50	55	65	65	50
RF Power (Watts)	1400	1400	2000	1800	800
Min BV_{DSS} (Volts)	135	177	203	179	170
Coss @ V_{DS} (Typ) pF	213	193	181	203	1000
VSWR Withstand	65:1	65:1	65:1	65:1	70:1
Swing Voltage / Safety Margin	2.7	3.5	3.1	2.8	3.4

Fig. 1: Comparison of rugged 50 V / 65 V Si LDMOS in comparison to Si VDMOS

The ART1K6 and ART2K0 are offered in industry standard packages, either air-cavity ceramic or over-mold plastic packages suitable for attach direct to an amplifier heatsink or copper-coin planar with PCB with gull-winged packages. Class-E designs are enabled at 50 V for ART2K0. Device is within all operating limits of up to 6dB compression. Testing underway to extend Class E operation at 50 V to 10 dB compression.

All ART Family devices have an internal stability network contained in the die. This network results in close to unconditional small signal stability at low frequency without the need for any external circuitry.

ART2K0: V_{DS} ~ 65 V | P_{OUT} ~ 2 kW | G_p ~ 25 dB | Drain Efficiency < 85 %

SOT539A (**ART2K0FE**)

ART1K6: V_{DS} ~ 50 V | P_{OUT} ~ 1.4 kW | G_p ~ 25 dB | Drain Efficiency < 85 %

SOT539A (**ART1K6FH**)

Fig. 2: ART Si LDMOS transistor products

ART Transistor Reference Designs

ART Transistors are demonstrated in various reference designs to showcase performance under various application and frequency requirements. The matrix below shows the existing reference designs, and more are in the works.

Fig. 3: Wire-wound, Ferrite Core Balun (re-position to ART192168)

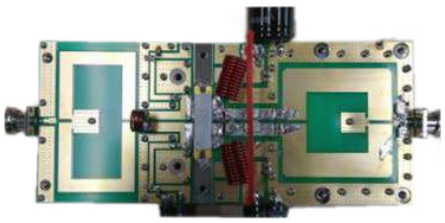

Fig. 4: 64 MHz Planar Balun (re-position to ART201106)

Fig. 5: 13 MHz and 27 MHz Binocular Balun HPA

Device Type	Application Report #	Frequency (MHz)	P_{OUT} (W)	Efficiency (%)	Application
ART2K0FE	AR192168	13	2000 (pulse)	82	Plasma Gen
ART2K0PE	AR212070	13	1700	>80	Plasma Gen
ART2K0FE	AR192168	27	1900 (pulse)	70	Plasma Gen
ART2K0PE	AR212040	27	1700	81	Plasma Gen
ART2K0FE	AR201104	41	1600	78.5	Plasma Gen
ART2K0FE	AR201024	41	1600	79	Plasma Gen
ART2K0FE	AR194008	60	> 1800 (pulse)	> 82	Plasma Gen
ART2K0FE	AR201106	64	2100	> 80	MRI
ART2K0FE	AR211018	81	1750	> 80	CO_2 Laser
ART2K0FE	AR192069	128	1900 (pulse)	65 / 75	MRI
ART2K0FE	AR201203	325	1600	75	Scientific
ART1K6PH	AR201041	325	1500	> 73	Scientific
ART2K0PE	AR201203	352	1600	75	Scientific
ART2K0PE	In Progress	433	1500 (pulse)	65	Medical

Fig. 6: Single Frequency Reference Designs

Device Type	Application Report #	Frequency (MHz)	P_{OUT} (W)	Efficiency (%)	Application
ART1K6FE	AR212082	2-30	1000	60	
ART2K0FE	AR201008	13-41	> 1100	> 55	Plasma
ART2K0FE	AR192131	20-100	> 1300	> 58	Comm's / EW
ART2K0FE	AR201042	88-108	1700	83	FM Broadcast
ART1K6FH	AR211050	88-108	1200	> 82	FM Broadcast
ART2K0FE	AR201083	170-240	> 250 P_{AVG} 1400 P_{PEAK}	> 45	Doherty for VHF TV
ART2K0PE	In Progress	400-450	1400 (pulse)	60	Radar

Fig. 7: Multi- Frequency Reference Designs

Driver Devices for ART Transistors

To allow for common voltage rail between driver and output transistor, Ampleon released 65 V ART drivers at 150 W and 35 W (ART150 and ART35). These driver transistors offer the same ruggedize features in an industry standard package to support necessary amplifier topology. Further, Ampleon offers a range of low cost, TO-270 packaged 50 V drivers in our BLP15H series, based on GEN9HV with SWVR of at least 40:1.

SOT467C Package

TO-270 Packages

Part Number	V_{DD} (V)	P_{OUT} (W)	G_p (dB)	Package
ART150FE	65-50	150	28[1]	SOT467C
ART35FE	65-50	35	28[1]	SOT467C
BLP15H9S010S	50	10	24[2]	TO-270
BLP15H9S030S	50	30	24[2]	TO-270
BLP15H9S100S	50	100	24[2]	TO-270

[1] @10-54 MHz
[2] @VHF

Fig. 8: Driver Device Reference Designs

Device Type	Application Report #	Frequency (MHz)	P_{OUT} (W)	Efficiency (%)	Application
ART150FE	AR201141	64	200 (pulse)	79	MRI, CO_2 Laser
ART150FE	AR201142	128	180	76	MRI
ART150FE	AR211048	128	160	84	MRI
ART150FE	AR211049	64	160	82	MRI
ART150FE	AR201141	100-140	190 170 (wide)	75	MRI, CO_2 Laser
ART35FE	AR201140	10-54	45	80	Plasma Gen
ART35FE	AR201131	60-130	50	81	MRI / Plasma

Fig. 9: Driver device reference designs at 65 V

ART2K0FE (2kW Si LDMOS Transistor) Applied in a 13 MHz Reference Design (AR#192168)

The 13 MHz amplifier design utilizes a balun transformer combiner with lumped elements deployed with ART2K0FE mounted on a Taconic 30RF35, 30 mm thick, 1 oz copper cladded printed circuit board material with a heatsink sweat soldered under the PCB. We utilized an even-mode stability network applied to the gate side of the amplifier.

The transfer plots demonstrate gain, power and efficiency under 10 %, 20 % and 50 % duty cycle conditions. The gain plots show an abundance of stable gain at 13 MHz with flat gain expansion over wide P_{OUT} levels. Thermal compression is more prevalent under saturated conditions at the 50 % duty cycle versus 20 % and 10 % as would be expected. The performance achieve at 62 V Vdd is G_p > 28.5 dB, P_{3dB} > 2 kW while achieving > 80 % at P_{satt}.

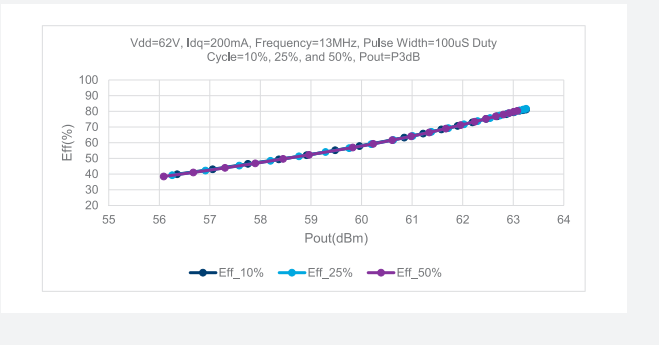

Fig. 10: (Swept Duty Cycle) drain efficiency (%) as a function of P_{OUT} (dBm)

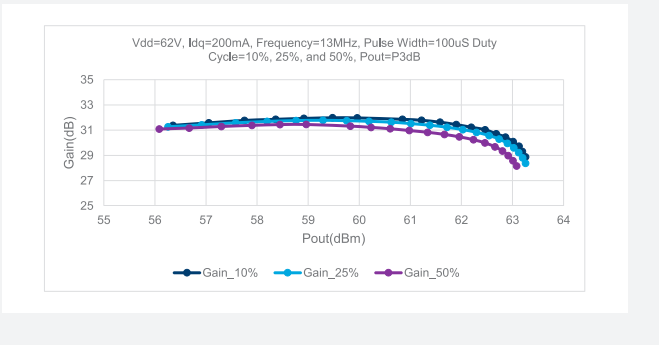

Fig. 11: (Swept Duty Cycle) gain (dB) as a function of P_{OUT} (dBm)

ART2K0FE (2 kW Si LDMOS Transistor) Applied in a 64 MHz Reference Design (AR#201106)

This 64 MHz amplifier utilizes a coplanar balun fabricated integral in the PCB. This allows for high power combining capabilities in a production-friendly and repeatable PCB fabrication process. This amplifier demonstrates P_{OUT} levels > 2180 W at 80 % P_{sat} efficiency while delivering power gain of 27 dB.

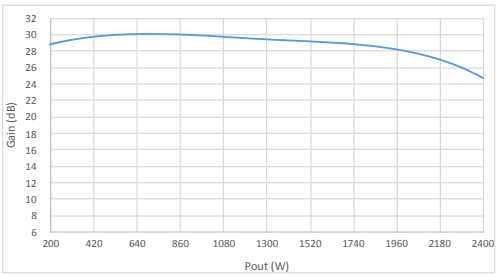

Fig. 12: 63 V pusled gain vs P_{OUT} (10 µs 20 %)

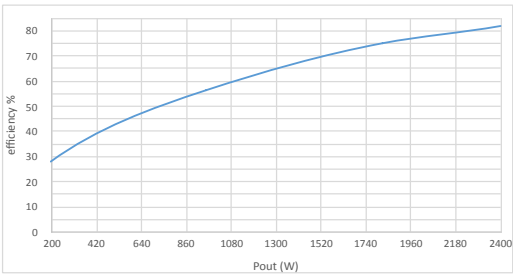

Fig. 13: 63 V pusled gain vs efficiency (10 µs 20 %)

ART Value Proposition

The value proposition for ART Si LDMOS transistors can be considered in two dimensions: either competitive Si LDMOS or competitive VDMOS. In each case, the ART transistors have compelling advantages.

Comparing to competitive 50 V / 65 V Si LDMOS

- The highest V_{DS} breakdown on the market, supportive of most rugged VSWR mismatch condition and offers best margin of safety for 50 Ohm and sub-50 Ohm mismatch conditions
- Higher gain, supports low cost, low power driver stages with 2-3 dB more power gain
- Higher Power: 10 % more output power

Comparing to competitive 50 V Si VDMOS

- Higher output power: 2.5 x more output power which allows for more scalable towards double-digit kilowatt powered HPAs. 2.5 x few devices split & combined to achieve necessary power. This is a significant SWaP feature
- Higher gain: 7-8 dB more power gain which allows for lower power drive power levels
- Higher efficiency: a significantly more efficient performance by almost a factor of 2 x (45 % VDMOS vs 80 % LDMOS). This is significant on many levels

System advantages 50 V Si VDMOS

- Power supply DC power levels 2 x less with LDMOS
- Thermal management dissipated power levels 4 x less with LDMOS
- Operational costs for industrial applications which operate 24 hours a day / 7 days a week: the operational cost saving of a LDMOS amplifier is half compared to VDMOS. This can approach $ 10 K of utility bill saving per amplifier on an annual basis

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